

October 1987 Revised August 2000

CD4023BC Buffered Triple 3-Input NAND Gate

General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to $V_{\rm DD}$ and $V_{\rm SS}$.

Features

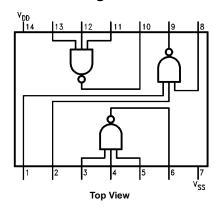
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ)
- Low power TTL compatibility: fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 µA at 15V over full temperature range

Ordering Code:

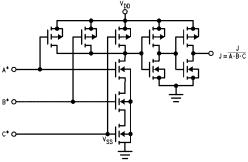
Order Number	Package Number	Package Description
CD4023BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
CD4023BCS	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4023BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" tot he ordering code.

Connection Diagram



Block Diagram



1/3 Device Shown

^{*}All Inputs Protected by Standard CMOS Input Protection Circuit.

Absolute Maximum Ratings(Note 1)

(Note 2)

 $\begin{array}{ll} \text{DC Supply Voltage (V}_{\text{DD}}) & -0.5 \text{ V}_{\text{DC}} \text{ to } +18 \text{ V}_{\text{DC}} \\ \text{Input Voltage (V}_{\text{IN}}) & -0.5 \text{ V}_{\text{DC}} \text{ to V}_{\text{DD}} +0.5 \text{ V}_{\text{DC}} \\ \text{Storage Temp. Range (T}_{\text{S}}) & -65^{\circ}\text{C to } +150^{\circ}\text{C} \end{array}$

Power Dissipation (P_D)

Dual-In-Line 700 mW Small Outline 500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions

 $\begin{array}{ll} \text{DC Supply Voltage (V}_{\text{DD}}) & 5~\text{V}_{\text{DC}}~\text{to 15 V}_{\text{DC}} \\ \text{Input Voltage (V}_{\text{IN}}) & 0~\text{V}_{\text{DC}}~\text{to V}_{\text{DD}}~\text{V}_{\text{DC}} \\ \text{Operating Temperature Range (T}_{\text{A}}) & -40^{\circ}\text{C to +85}^{\circ}\text{C} \end{array}$

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
Syllibol	rarameter	Conditions	Min	Тур	Min	Тур	Max	Min	Max	Units
I _{DD}	Quiescent Device Current	$V_{DD} = 5V$		1.0		0.004	1.0		7.5	
		$V_{DD} = 10V$		2.0		0.005	2.0		15	μΑ
		$V_{DD} = 15V$		4.0		0.006	4.0		30	
V _{OL}	LOW Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
V _{OH}	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
V _{IL}	LOW Level Input Voltage	V _{DD} =5V, V _O =4.5V		1.5		2	1.5		1.5	
		V_{DD} =10V, V_{O} =9.0V $ I_{O} $ <1 μ A		3.0		4	3.0		3.0	V
		V _{DD} =15V, V _O =13.5V		4.0		6	4.0		4.0	
V _{IH}	HIGH Level Input Voltage	V _{DD} =5V, V _O =0.5V	3.5		3.5	3		3.5		
		V_{DD} =10V, V_{O} =1.0V $ I_{O} $ <1 μ A	7.0		7.0	6		7.0		V
		V _{DD} =15V, V _O =1.5V	11.0		11.0	9		11.0		
l _{OL}	LOW Level Output Current	$V_{DD} = 5V, V_{O} = 0.4V$	0.52		0.44	0.88		0.36		
	(Note 4)	$V_{DD} = 10V, V_{O} = 0.5V$	1.3		1.1	2.2		0.90		mA
		$V_{DD} = 15V, V_{O} = 1.5V$	3.6		3.0	8		2.4		
I _{OH}	HIGH Level Output Current	$V_{DD} = 5V, V_{O} = 4.6V$	-0.52		-0.44	-0.88		-0.36		
	(Note 4)	$V_{DD} = 10V, V_{O} = 9.5V$	-1.3		-1.1	-2.2		-0.90		mA
		$V_{DD} = 15V, V_{O} = 13.5V$	-3.6		-3.0	-8		-2.4		
I _{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10 ⁻⁵	-0.3		-1.0	μА
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10 ⁻⁵	0.3		1.0	μА

Note 3: V_{SS} = 0V unless otherwise specified.

Note 4: \mathbf{I}_{OH} and \mathbf{I}_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)

 $T_A = 25^{\circ}C,\, C_L = 50$ pF, $R_L =$ 200k, unless otherwise specified

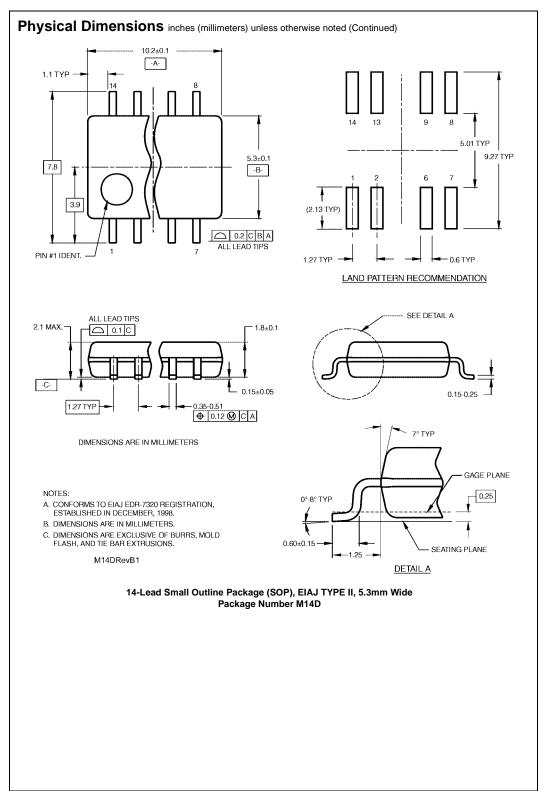
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{PHL}	Propagation Delay, HIGH-to-LOW Level	$V_{DD} = 5V$		130	250	
		$V_{DD} = 10V$		60	100	ns
		$V_{DD} = 15V$		40	70	
t _{PLH}	Propagation Delay, LOW-to-HIGH Level	$V_{DD} = 5V$		110	250	
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		35	70	
t _{THL} ,	Transition Time	$V_{DD} = 5V$		90	200	
t _{TLH}		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	
C _{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C _{PD}	Power Dissipation Capacity (Note 6)	Any Gate		17		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics Application Note AN-90.

Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.335 - 0.344}{(8.509 - 8.738)}$ LEAD NO. 1 IDENT 0.010 MAX (0.254) $\frac{0.150 - 0.157}{(3.810 - 3.988)}$ $\frac{0.053 - 0.069}{(1.346 - 1.753)}$ $\frac{0.010 - 0.020}{(0.254 - 0.508)}$ 8° MAX TYP ALL LEADS $\frac{0.004 - 0.010}{(0.102 - 0.254)}$ SEATING PLANE 0.014 0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS 0.050 (1.270) TYP $\frac{0.014 - 0.020}{(0.356 - 0.508)} \text{ TYP}$ 0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS 0.004 (0.102) ALL LEAD TIPS 0.008 (0.203) TYP M14A (REV h)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.620 - 8.128}{(7.620 - 8.128)}$ 0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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8.255 + 1.016

N144 (REV.F)

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